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A Self-Test and Self-Repair Approach for Analog Integrated Circuits

Mouna Karmani
Electronics & Microelectronics Laboratory
Monastir, Tunisia
mouna.karmani@yahoo.fr

Tomas Krilavičius
Vytautas Magnyus University - Lithuania and
Baltic Institute of Advanced Technology - Lithuania
t.krilavicius@bpti.lt

Chiraz Khedhiri
Electronics & Microelectronics Laboratory
Monastir, Tunisia
chirazkhedhiri@yahoo.fr

Belgacem Hamdi
Electronics & Microelectronics Laboratory
Monastir, Tunisia
ISSAT, Sousse – Tunisia
Belgacem.Hamdi@issatgb.rnu.tn

Ka Lok Man
Xi'an Jiaotong-Liverpool University – China
ASIC LAB, Myongji University – South Korea and
Baltic Institute of Advanced Technology – Lithuania
ka.man@xjtlu.edu.cn

Amir-Mohammad Rahmani
Department of Information Technology
University of Turku, Finland
amir.rahmani@utu.fi

***Abstract*— With the continuous increase of integration densities and complexities, secure integrated circuits (ICs) are more and more required to guarantee reliability for safety-critical applications in the presence of soft and hard faults. Thus, testing has become a real challenge for enhancing the reliability of safety-critical systems. This paper presents a Self-Test and Self-Repair approach which can be used to tolerate the most likely defects of bridging type that create a resistive path between V_{DD} supply voltage and the ground occurring in analog CMOS circuits during the manufacturing process. The proposed testing approach is designed using the 65 nm CMOS technology. We then used an operational amplifier (OPA) to validate the technique and correlate it with post layout simulation results.**

Keywords- Analog ICs; Self-test; Self-repair; Built-In Current Sensor (BICS); Bridging faults; 65 nm CMOS technology;

I. INTRODUCTION

The constant advances in VLSI technology have given the capability to design and manufacture very complex integrated circuits that include digital, analog and mixed circuits in the same chip. The approach based on integrating all these components into a single chip is known as the system-on-a chip (SoC) approach design [1-2]. Although this approach simplifies the design phase of the product, it increases the complexity of testing of the system, in particular testing of the analog blocks or analog functions embedded in mixed-signal or analog cores [2].

With the rapid increase of chip complexity in computer and communication industries, testing of electronic components is a real challenge and an important part of the business to ensure the functionality and quality of a reliable product at a reasonable cost [3]. Distinguishing between faulty and fault-free ICs is a challenging task. It is also one of the crucial tasks in design and manufacturing of integrated circuits.

The traditional tests are the most expensive in terms of both test development costs and implementation for analog and mixed signal circuits. In a SoC, up to 80% of the test cost is due to the analog and mixed signal functions that typically occupy only around 10% of the chip area [4].

The conventional testing methods based on specifications and using automatic test equipment are known to be time consuming and expensive. In addition, there are many problems with analog circuits such as the node accessibility problems and the lack of common test strategies and standards. Therefore, due to those difficulties, self-test techniques for analog and mixed signal blocks are gaining importance [5-6]. In fact, self–testing is the technique of designing additional hardware features into integrated circuits to enable them to perform self-testing and thereby reducing dependence on external automated test equipment (ATE). Thus, the self-testing approach is a Design-for-Testability (DFT) technique to provide simpler, faster, more efficient, and cost-effective testing of a chip [7].

Developing a self-testing approach that reduces test cost and accelerates time-to-market without exacerbating the quality of the IC is too challenging because the quality of the test methodology has direct consequences on the price and the quality of the final product [8]. This work proposes a fault-tolerant technique which can detect and correct hard faults. In this paper, we propose a Self-Testing and Self-repair methodology based on the use of a Built-In current Sensor (BICS) that enables the detection of faults in analog circuits.

The proposed self-repair approach based on online testing is able to tolerate hard faults. The goals of this approach are to ensure the correctness of the system operation, to extend the component lifetime, and to improve the yield. The Self-Repair property presented in this work is based on hardware redundancy.

The most of existing self-test and self-repair approaches for analog integrated circuits are based on using a Built-In Current Sensor (BICS) to control the I_{DDQ} current of the circuit under test. In fact, each fault which increases the I_{DDQ} current will be detected using the BICS and immediately corrected by hardware redundancy using a fault-free circuit and an analog multiplexer.

To prove the efficiency of the proposed technique, a full custom CMOS operational amplifier is implemented in 65 nm CMOS technology. Then, the most likely faults of bridging type, that create a resistive path between V_{DD} supply voltage and the ground are deliberately injected in the layout.

The paper is organised as follows. Section II presents the self-test and self-repair approach for analog integrated circuits, while a case study is presented in Section III. Finally, Section IV concludes this paper.

II. The Built-In Self-Test and Repair Approach

The general block diagram of the proposed approach is shown in Fig. 1.

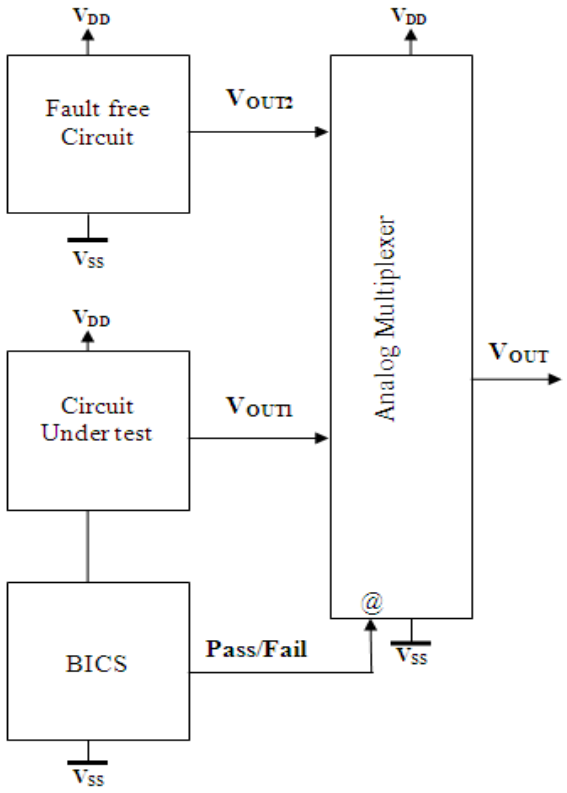

Figure 1. The proposed self-test and self-repair approach

The self-test and self-repair methodology presented in this paper is based on using a BICS to control the leakage current of the circuit under test (CUT). The BICS is used to detect the presence of multiple bridging faults that create a direct path between V_{DD} and V_{SS}. The BICS output is a *Pass/Fail* signal. In fact, when a fault causing an elevated I_{DDQ} leakage current occurs, the output of the BICS must be equal to the high level (*Fail*). Otherwise, the CUT is fault-free and the BICS output must be equal to the low level (*Pass*). The fault-free analog output (V_{out2}) is obtained by hardware redundancy or it can be digitalized and pre-stored in a flash memory embedded in the considered SoC.

The built-in self-repair concept presented in this work uses hardware redundancy. For the chip manufacturer, the self-test procedure can help to simplify the device characterization process by providing greater visibility into the device and can reduce manufacturing test time by allowing autonomous testing of some subset of the chip.

In the next section, we present the I_{DDQ} test technique that serves to test analog ICs, and distinguish a fault-free from a faulty circuit with respect to short (bridging) defects. This technique is based on analysing the leakage current (I_{DDQ}) of the circuit under test using a Built-In Current Sensor. In our investigation, we show that at the nanometer range (the 65 nm node) I_{DDQ} testing can be used to detect multiple bridging defects which create a resistive path between V_{DD} supply and the ground.

I_{DDQ} test is based on measuring the current on supply lines (V_{DD}, *GND*) of the circuit under test. The defects which increase the I_{DDQ} current are detected using a BICS inserted between the circuit under test and the ground. For CMOS technologies which are of the micro-meter order, a single short between two nodes in the circuit can increase significantly the I_{DDQ} current. Thus, the BICS can easily detect the presence of the fault [2-9]. However in [2] the authors show that at the nano-meter range (90 nm and below) the I_{DDQ} testing is used to diagnose only the multiple bridging faults being able to create a resistive path between V_{DD} and ground. Consequently, for the 65nm node technology, this testing approach will be appropriate only with respect to the multiple short faults occurring in the circuit under test and creating a resistive path between the power supply voltage and the ground.

Fig. 2 shows the detailed design of the Built-In Current Sensor inserted between the CMOS circuit under test and the ground [10].

Using the BICS requires the estimation of the reference current I_{REF} which is the I_{DDQ} current value of the fault-free integrated circuit under test. Then, while testing the circuit, if the I_{DDQ} current of the circuit under test is equal or less than I_{REF}, it is supposed that the circuit is fault-free, otherwise, the increase in current beyond this value means that there is a failure in the circuit [2-10].

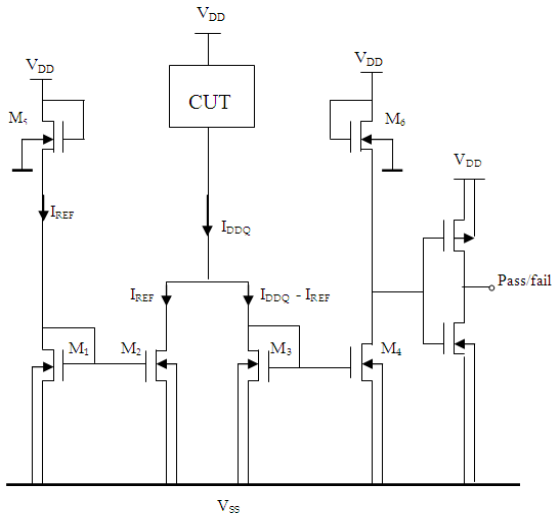

Figure 2. The detailed Built-In Current Sensor CMOS design

III. CASE STUDY

In order to evaluate the efficiency of the proposed test technique, we apply the above mentioned test procedure to a CMOS Operational Amplifier (OPA) circuit.

A. *CMOS Operational Amplifier*

The CMOS Operational Amplifier under test is a two-stage amplifier including a differential input amplifier and single-ended output stages. A floor conversion following the differential amplifier stage is responsible for producing a single output which is referenced to the ground. Fig. 3 shows the circuit of the open loop CMOS operational amplifier.

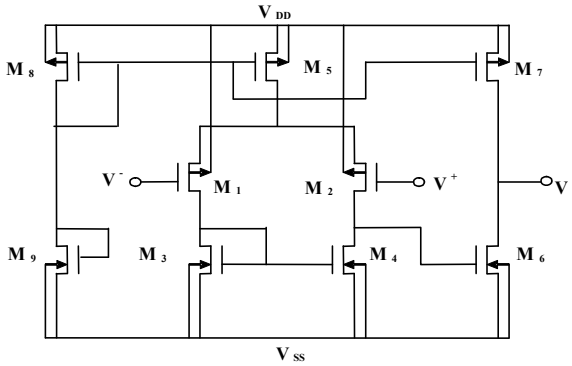

Figure 3. The CMOS operational amplifier

The transistors are sized to have a bias current of 29μA intensity and an amplifier's quiescent current I_{DDQ} equal to 140μA. The operational amplifier is implemented in full-custom 65nm CMOS technology [11]. For this technology, the appropriate supply voltage V_{DD} is equal to 1V while V_{SS} is the ground (*GND*). SPICE simulations of the post-layout extracted OPA, which includes all parasitic, are used to demonstrate that this amplifier has an acceptable electrical behaviour. The layout of the amplifier is as shown in Fig. 4.

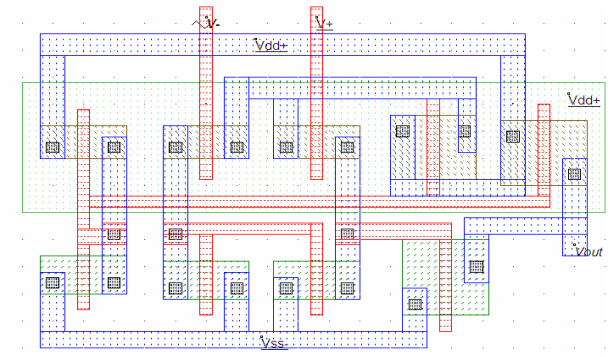

Figure 4. Layout of the operational amplifier in full-custom 65 nm CMOS technology

The bias current and the I_{DDQ} current of the Op amp are illustrated in Fig. 5.

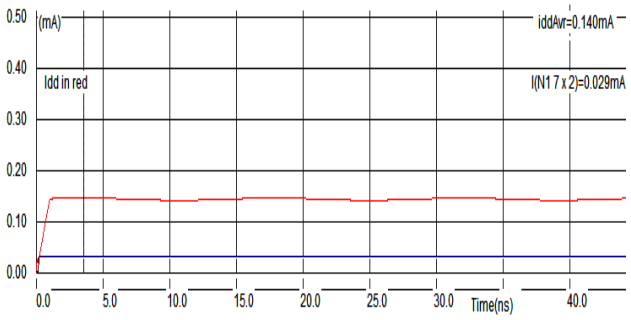

Figure 5. The bias current and the I_{DDQ} current of the fault-free OPA

Fig. 5 shows the bias current and the I_{DDQ} current of the fault-free OPA circuit. The bias current is equal to 29μA and the average value of the I_{DDQ} current is equal to 0.14mA, as expected.

B. *Physical Defects in CMOS Analog Integrated Circuits*

In analog CMOS technology, faults are further classified into catastrophic (open and bridging) and parametric faults. When a catastrophic defect occurs, the topology of the circuit is changed. In fact, a bridging defect is a short circuit between two or more nets on a die [12-13]. While an open circuit defect can occurs as a result of missing metal material in the transistor interconnects.

The set of faults to be tested is previously defined. This set contains typical parametric and catastrophic faults. The set of faults to be considered is the most likely faults type short circuit (bridging) occurring during the manufacturing process of ICs. To prove the efficiency of the proposed technique, the most likely faults which can induce the failure of the system are deliberately injected and simulated at the layout level of the implemented custom sub circuit under test (CMOS operational amplifier), i.e. we will inject some probable faults type short defects (bridging faults) in the OPA. Each Bridging fault is placed in the CMOS amplifier design using a fault injection NMOS transistor (FIT). More precisely, when the gate of the fault injection transistor is connected to V_{DD}, the FIT is activated and consequently the defect is injected. Otherwise, the FIT is turned off and the fault is not injected.

Now, we inject a resistive path between V_{DD} and V_{SS} supply in the circuit under test. This fault consists of injection of two short defects at the same time in the circuit under test in order to obtain a resistive path. The first short defect is injected between the source and the gate of the *PMOS* M_8 transistor and the second is injected between the source and the gate of the *NMOS* M_9 transistor. Thus, in order to inject the resistive path 1, we must use two fault injection transistors (FIT_1 and FIT_2) as shown in Fig. 6.

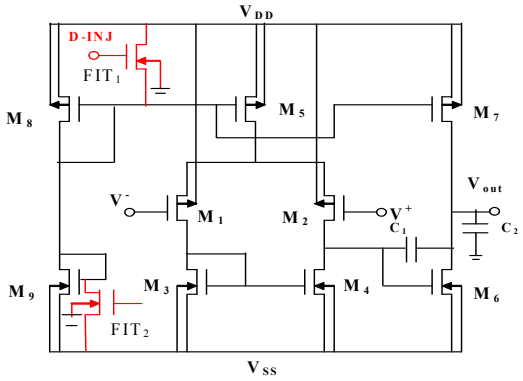

Figure 6. The resistive path created using two fault injection transistors

Fig. 7 shows the simulation results of the implemented self-test and self-repair design obtained by injecting the resistive path at the layout level.

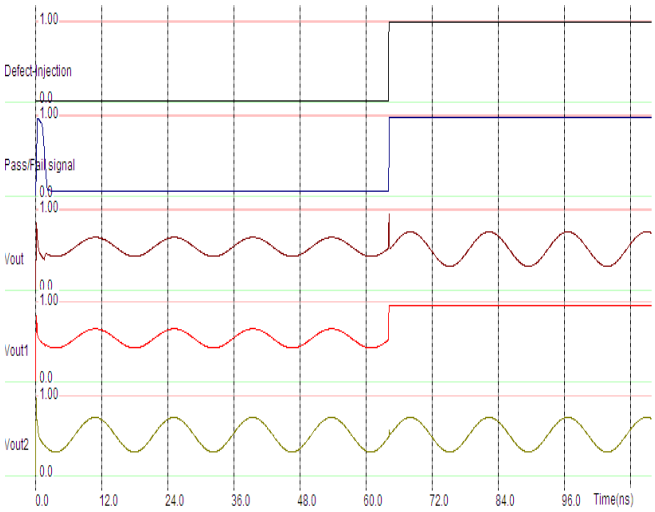

Figure 7. Simulation results of the implemented self-test and self-repair design

As can be seen from Fig. 7, the BICS is sensitive to the resistive path injected in the circuit under test. In fact, when the CUT is fault-free (*defect-injection = 0*) the output of the BICS is *Pass* (low level) and the multiplexer output is equal to V_{out1}. Otherwise, when the circuit is faulty (*defect-injection = 1*) the output of the BICS is *Fail* (high level) and the multiplexer output switches from the faulty output to the fault-free one and it will be equal to V_{out2}. Therefore, the proposed self-test and self-repair approach is effective since the considered resistive path caused by the two bridging faults injected in the CUT is not only detected by the BICS but it is also immediately corrected by the hardware redundancy based self–repair technique.

IV. Conclusion

For analog and mixed signal ICs, testing is one of the major cost factors in the overall IC manufacturing costs. Hence, developing testing approaches that reduce test cost and accelerate the time-to-market without sacrificing IC quality is too challenging. In this paper, we presented a self-test and self-repair methodology to ensure product quality and reliability for devices that are in the nanometer technology range. This approach is based on using a Built-In Current Sensor to ensure the on-line detection of the most likely defects of multiple bridging faults type occurring in analog CMOS circuits during the manufacturing process and creating a resistive path between the power supply voltage V_{DD} and the ground. In this approach, when a fault is detected, the self-repair property is immediately ensured by hardware redundancy. Simulation results show that the proposed testing technique is effective and minimises the need of using expensive testers. It also offers a solution for testing critical sub-circuits that have no direct connections to external pins.

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